Notice of Allowability	Application No. 09/658,597	Applicant(s) LARKY ET AL.
	Examiner Jeffrey R. West	Art Unit 2857

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the After Final Response filed 24 March 2005*.

2. ☒ The allowed claim(s) is/are *1-8 and 10-26*.

3. ☒ The drawings filed on *09 September 2002* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

PATRICK ASSOUAD
PRIMARY EXAMINER

DETAILED ACTION

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Mr. Christopher P. Maiorana on April 21, 2005.

3. The application has been amended as follows:

In claim 15, line 2, "speed" has been changed to ---speed from a low speed tester---.

In claim 15, line 3, "interface" has been changed to ---interface of a host emulator---.

In claim 15, line 4, "a test packet" has been changed to ---a first test packet---.

In claim 15, line 5, "interface" has been changed to ---interface of said host emulator---.

In claim 15, line 9, "a signal" has been changed to ---a first done signal---.

In claim 15, line 10, "interface" has been changed to ---interface of said host emulator---.

Allowable Subject Matter

4. Claims 1-8 and 10-26 are considered to be allowable over the cited prior art for the following reasons.

Catalyst Enterprises, Inc., "SBAE-10" Bus Analyzer-Exerciser User's Manual and Analyzer/Exerciser/Tester specification sheet (henceforth "Catalyst") discloses, with respect to claims 1, 15, and 16, an apparatus comprising a low speed tester (i.e. windows based system) and a host emulator (i.e. SBAE-10) having a first bi-directional interface (i.e. parallel port) coupled to said low speed tester to receive test data at a first speed (User's Manual, page 6, Figure 3), (ii) a second interface (i.e. primary USB connector) configured to (a) transmit said test packet to a device and (b) receive a response packet from said device (User's Manual, page 32-33) and (iii) transferring on the bi-directional interface to said low speed tester for display a first done signal (i.e. error signal and result signals) based upon said response (User's Manual, page 14, page 49, lines 1-2 and page 51, lines 1-4).

With respect to claim 2, Catalyst discloses that said host emulator is further configured to perform a verification of said device (Specification Sheet, page 1, column 1, User's Manual, page 2, "Basic Analyzer", and User's Manual, page 33, verify that target received data without error).

With respect to claims 3 and 17, Catalyst discloses that said device comprises a Universal Serial Bus (USB) device (User's Manual, page 6, Figure 3).

With respect to claims 5 and 18, Catalyst discloses that said low speed tester is configured to control said host emulator through a GUI (User's Manual, page 23, Figures 19-20 and page 32).

With respect to claims 8 and 10, Catalyst also teaches a tester function to control the apparatus/host emulator to initiate test packets for a transmission/reception loop as well as verifying the packets or forcing packet errors to the USB device for correct operation verification (User's Manual, page 14, Time Out detection, page 33, acknowledge that device received data without error, and pages 39-40).

With respect to claims 11, 12, and 25, Catalyst discloses that under control of the host emulator that transmits a first packet, said device initiates the transmission of a response packet that is then received and verified by the host emulator to determine if a time constraint has been met (User's Manual, page 14 and pages 32-33).

With respect to claims 14 and 20, Catalyst discloses that said apparatus is configured to perform at least one test of a plurality of test modes (User's Manual, pages 17-18) wherein said plurality of test modes comprise USB 2.0 defined test modes (Specification Sheet, page 1, lines 1-2) in production environments (i.e. devices undergoing a debugging stage) (User's Manual, page 2, lines 1-4).

With respect to claims 21 and 23, Catalyst discloses that said host emulator is configured to generate said first done signal (i.e. error signal) to indicate no successful reception of said test packet within said predetermined time (i.e. Time Out) (User's Manual, page 14).

Further, while the invention of Catalyst teaches performing full and low-speed testing of the device under test by receiving first signals from the low-speed tester over a parallel connection to the host emulator which performs the low and full-speed testing of the device under test over a USB connection (Catalyst, User's Manual, page 6), Catalyst does not explicitly state that the emulator transmits test data at a second speed faster than the first speed received from the low-speed tester.

It can be argued that, due to the well-known maximum data transfer rates of parallel ports, USB ports and the requirements of low and full-speed testing, the speed of the test data transmitted by the host emulator to perform the low and full-speed testing must be faster than the test data sent from the windows based system. While this position is not certain, any proposed modification to the invention of Catalyst to modify the bidirectional interface between the windows based system and host emulator would destroy any suggested inherency regarding the data transmission speeds, since Catalyst does not explicitly define the windows based system to be at a speed lower than that of the host emulator and such modification would eliminate the bidirectional interface along with any inherent properties thereof. Further, one having ordinary skill in the art would recognize that in modifying the bidirectional interface to be two separate interfaces would also include modifying the windows based system to transmit test data at the desired high speeds to reduce the requirement of the host emulator to speed-up the test data.

U.S. Patent No. 5,177,630 to Goutzoulis et al. teaches a method and apparatus for generating and transferring high speed data for high speed testing applications by generating and transferring low-speed input vectors (i.e. vectors at a first speed) from an external test vector generator to the test device which configures the device by triggering specific components to adjust the delay (column 1, lines 34-40 and column 2, line 60 to column 3, line 7) and generate high-speed test vectors (i.e. vectors at a second speed faster than said first speed) for transferring the high-speed test vectors to a digital DUT (column 2, lines 50-54).

U.S. Patent No. 5,959,911 to Krause et al. teaches an apparatus and method for implementing a bank interlock scheme and related test mode for multi-bank memory devices including data lines for transmitting read and write data (column 2, lines 49-59), wherein the read and write lines can either be implemented as separate lines with separate interfaces or a bi-directional line with one interface (column 3, lines 13-15).

U.S. Patent No. 6,304,982 to Mongan et al. teaches a network distributed automated testing system including a test computer that receives error message responses resulting from a test (column 2, lines 19-21) and makes a decision for a pass/fail condition of the test based on said response to generate a pass/fail signal indicating the decision to a display (column 2, line 61 to column 3, line 8 and column 3, lines 12-16).

U.S. Patent No. 5,583,874 to Smith et al. teaches a 10Base-T portable link tester including a test device that asserts a done signal through a discrete output to light an LED in response to successfully receiving a test vector from a PC host (column 2, lines 9-25, column 4, lines 46-52 and column 5, lines 40-64).

As noted above, the cited prior art teaches many of the features of the claimed invention. None of the cited prior art teaches or suggests, however, in combination with the other claimed limitations, an apparatus including, or a method for, a host emulator, as opposed to a target or environment emulator, having a first interface coupled to a low speed tester to receive a test vector at a first speed, a second interface configured to transmit a first test packet to a device at a second speed faster than said first speed and receive a response from said device, and a third interface to said low speed tester to transfer a first done signal based upon said response, as part of an apparatus configured to allow said low speed tester to perform high speed tests of said device at said second speed.

The further newly discovered art is considered pertinent to the examination of the instant application for disclosure of relevant subject matter:

U.S. Patent No. 5,946,472 to Graves et al. teaches an apparatus and method for performing behavioral modeling in hardware emulation and simulation environments including a behavior card that receives test vectors from a workstation at a first

speed over a first interface, transmits data to a target hardware at a second speed, faster than said first speed, and receives a response from the target hardware over a second interface, and transmits results to the workstation over said first interface.

Graves at al. does not include a third interface or specify the transmission of a first done signal. Graves also does not define the behavior card as a "host emulator" and further teaches away from using a host emulator as the behavior card since Graves specifically includes a hardware emulator in separate embodiments.

U.S. Patent No. 5,475,624 to West teaches test generation by environment emulation.

U.S. Patent No. 5,049,814 to Walker et al. teaches testing of integrated circuits using clock bursts.

U.S. Patent No. 4,901,259 to Watkins teaches an ASIC emulator.

U.S. Patent No. 5,410,547 to Drain teaches a video controller IC with built-in test circuit and method of testing.

U.S. Patent No. 6,571,357 to Martin et al. teaches a high-speed device emulation computer system tester.

U.S. Patent Application Publication No. 2001/0047253 to Swoboda teaches a data processing condition detector with table lookup.

U.S. Patent No. 6,535,831 to Hudson et al. teaches a method for sourcing three level data from a two level tester pin faster than the maximum rate of a tester.

U.S. Patent No. 6,345,373 to Chakradhar et al. teaches a system and method for testing high-speed VLSI devices using slower testers.

U.S. Patent No. 5,951,704 to Sauer et al. teaches a test system emulator.

U.S. Patent No. 5,937,154 to Tegethoff teaches the manufacturing function testing of computing devices using microprogram based functional tests applied via the devices own emulation debug port.

U.S. Patent No. 5,889,936 to Chan teaches a high-speed asynchronous digital testing module.

U.S. Patent No. 5,778,004 to Jennion et al. teaches a vector translator.

U.S. Patent No. 5,581,742 to Lin et al. teaches an apparatus and method for emulating a microelectronic device by interconnecting and running test vectors on physically implemented functional modules.

FOLDOC: Free On-Line Dictionary of Computing, "host" and "emulation" defines a host as "A computer connected to a network" and emulation as "When one system performs in exactly the same way as another, though perhaps not at the same speed".

None of the newly discovered prior art teaches or suggests, however, in combination with the other claimed limitations, an apparatus including, or a method for, a host emulator, as opposed to a target or environment emulator, having a first interface coupled to a low speed tester to receive a test vector at a first speed, a second interface configured to transmit a first test packet to a device at a second speed faster than said first speed and receive a response from said device, and a third interface to said low speed tester to transfer a first done signal based upon said

response, as part of an apparatus configured to allow said low speed tester to perform high speed tests of said device at said second speed.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (571)272-2226. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571)272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jrw
April 25, 2005

PATRICK ASSOUAD
PRIMARY EXAMINER